REMARKS

Applicant respectfully requests reconsideration of the present application in view of this response. Claim 18 was previously canceled. Claims 1-17 and 19-33 are currently pending. Of those, claims 1, 17, 32 and 33 have been amended and are independent claims.

Allowable Subject Matter

Applicant acknowledges the Examiner's indication of allowable subject matter set forth in claims 5-9, 30 and 31. By way of this response, Applicant has amended claim 33 to correct the minor antecedent basis problem noted by the Examiner. Applicant submits that claim 33 is in condition for allowance.

Information Disclosure Statement

Applicant appreciates the Examiner's careful consideration of all references cited in the Information Disclosure Statement filed February 6, 2004 as indicated by the Examiner's initials and signature on the Form PTO-1449.

Rejection under 35 U.S.C. §112, 2nd Paragraph

As noted above, Applicant has amended claim 33 to correct the minor antecedent basis problem noted by the Examiner. Withdrawal of this rejection is kindly requested.

Rejection under 35 U.S.C. §102(b)

Claims 1, 2, 17, 26-28, 30 and 32 stand rejected under 35 U.S.C. §102(e) as allegedly being anticipated by Pan (U.S. Patent No. 6,734,718, hereinafter referred to as "Pan"). Applicant respectfully traverses this rejection.

On page 3 of the Office Action, the Examiner relies upon the current control circuit 450 in FIG. 4 of Pan to allegedly teach the "control circuit," of claim 1. In doing so, the Examiner relies upon the output of the current control circuit 450 to allegedly teach the "control current," of claim 1. Applicant disagrees.

FIG. 4 of Pan illustrates a charge pump. As shown, an input voltage V0 is boosted by each of a plurality of voltage multiplier stages 410, 420 and 430 to generate a boosted output voltage Vn. In doing so, a current control circuit 450 may configure the voltage multiplier stages 410, 420 and 430 in response to a signal output from a voltage detector 460. The voltage detector 460 outputs the signal according to the level of the output voltage Vn.

FIG. 2 is a more detailed illustration of one of the voltage multiplier stages 410, 420 and 430. As shown, the voltage multiplier stage of FIG. 2 receives two inputs, an input voltage Vn-1 and a clock signal CLK. As will be appreciated from FIG. 4, the input voltage is the input voltage V0 or an output voltage from the preceding voltage multiplier stage, and the clock signal CLK is output from the current control circuit 450.

FIG. 6 is a more detailed illustration of the voltage multiplier stage 430, according to another embodiment of Pan. As shown in FIG. 6, the current

control circuit 450 configures the voltage multiplier stage 430 via driver circuits 610, 620 and 630. FIG. 7 is a more detailed illustration of a driver circuit according to Pan. As shown, the current control circuit 450 outputs clock signals CLK to each of a plurality of transistors T1, T3 and T4 for controlling the current to be used boosting the voltage from V0 to Vn.

Contrary to the "control circuit," of claim 1, however, the current control circuit 450 of Pan does not output a "control current," but instead, **only outputs a clock signal CLK** to control the current output from the voltage multiplier stages 410, 420 and 430.

For at least these reasons, the current control circuit 450 of Pan is not the "control circuit," of claim 1, and the output of the current control circuit 450 is not the "control current," of claim 1. Thus, claim 1 is in condition for allowance.

Claim 32 is allowable for at least reasons somewhat similar to those set forth above with regard to claim 1.

Regarding claim 17, the Examiner relies upon the output of the current control circuit 450 to allegedly teach the "control current," of claim 17. However, contrary to the Examiner's allegation the current control circuit 450 merely outputs a clock signal CLK and not a "control current," as required by claim 1. For at least this reason, claim 17 is in condition for allowance.

Claims 2, 26-28 and 30 are allowable at least by virtue of their dependency from claim 1.

Rejection under 35 U.S.C. § 103(a)

The Examiner further rejects claims 3, 10-16 and 19-25 under 35 U.S.C. § 103(a) as allegedly being unpatentable over Pan in view of Bayer et al. (U.S. Patent No. 6,392,904, hereinafter referred to as "Bayer"). This rejection is respectfully traversed in that even assuming *arguendo* that Pan could be combined with Bayer (which Applicant does not admit), Bayer still fails to at least make up for the above described deficiencies of Pan with regard to claims 1 or 17.

Withdrawal of this rejection is kindly requested.

Rejection under 35 U.S.C. § 103(a)

The Examiner further rejects claims 3, 10-16 and 19-25 under 35 U.S.C. § 103(a) as allegedly being unpatentable over St. Pierre (U.S. Patent No. 6,208,196) in view of Pan. This rejection is respectfully traversed.

On page 6 of the Office Action, the Examiner acknowledges that St. Pierre fails to teach or suggest the "control circuit," of claim 1. The Examiner relies upon the current control circuit 450 of Pan to allegedly teach this feature. However, for at least the reasons discussed above with regard to claim 1, the current control circuit 450 of Pan is not the "control circuit," of claim 1. As such, even assuming *arguendo* that St. Pierre could be combined with Pan (which Applicant does not admit); the combination still fails to teach all features of claim 4. Thus, claim 4 is in condition for allowance. Claim 29 is

also allowable for reasons somewhat similar to those set forth above with regard to claim 4.

Withdrawal of this rejection is kindly requested.

CONCLUSION

In view of above remarks, reconsideration of the outstanding rejection and allowance of the pending claims is respectfully requested.

If the Examiner believes that personal communication will expedite prosecution of this application, the Examiner is invited to telephone the undersigned at number listed below.

If necessary, the Commissioner is hereby authorized in this, concurrent, and future replies to charge payment or credit any overpayment to Deposit Account No. 08-0750 for any additional fees required under 37 C.F.R. §§ 1.16 or 1.17; particularly, extension of time fees.

Respectfully submitted,

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